IN THE CLAIMS:

Please amend the claims as set forth below.

1-19 (Cancelled).

20. (New) A computer system comprising:

a first node configured to initiate a transaction by transmitting a request; and

a second node coupled to receive the request from the first node, wherein the second node is configured to generate a probe in response to the request, and wherein the probe includes an indication which designates a receiving node to receive responses to the probe, and wherein the receiving node is the first node responsive to the transaction having a first type, and wherein the receiving node is the second node responsive to the transaction having a second type.

21. (New) The computer system as recited in claim 20 wherein the probe comprises a packet including a command field identifying the packet as the probe, and wherein the indication is included within the command field.

22. (New) The computer system as recited in claim 20 further comprising a third node coupled to receive the probe.

23. (New) The computer system as recited in claim 22 wherein the third node is configured to generate a probe response, and wherein the third node is configured to route the probe response responsive to the indication.

24. (New) The computer system as recited in claim 20 wherein the second type is a write of a first number of bytes, the first number of bytes being less than a second number of bytes in a cache block of data.

25. (New) The computer system as recited in claim 24 wherein the first type is other than the write.

26. (New)The computer system as recited in claim 20 wherein the probe comprises a first packet including a target node field identifying the second node and a source node field identifying the first node.

27. (New) The computer system as recited in claim 26 further comprising a third node coupled to receive the probe and generate a probe response in response to the probe, and wherein the probe response comprises a second packet including a response node field, and wherein the third node is configured to use a value from the target node field of the first packet as the value in the response node field responsive to the indication designating the second node as the receiving node.

28. (New) The computer system as recited in claim 27 wherein the third node is configured to use a value from the source node field of the first packet as the value in the response node field responsive to the indication designating the first node as the receiving node.

29. (New) The computer system as recited in claim 20 wherein the second node comprises a memory controller configured to communicate with a memory in which the cache block is stored, and wherein the memory controller is configured to generate the probe in response to selecting the request to access the memory.

30. (New) A method for maintaining coherency in a computer system, the method comprising:

transmitting a request from a source node to a target node to initiate a transaction;

generating a probe in the target node responsive to the request; and

designating a receiving node for responses to the probe via an indication within the probe responsive to a type of the transaction, wherein the receiving node is the source node responsive to the transaction having a first type, and wherein the receiving node is the target node responsive to the transaction having a second type.

31. (New) The method as recited in claim 30 further comprising routing a probe response to the one or more probes to the receiving node.

32. (New) The method as recited in claim 30 wherein the second type is a write of a first number of bytes, the first number of bytes being less than a second number of bytes in a cache block of data.

33. (New) The method as recited in claim 32 wherein the first type is other than the write.

34. (New) A first node comprising a circuit coupled to receive a request generated by a second node to initiate a transaction, wherein the circuit is configured to generate a probe in response to the request, and wherein the probe includes an indication which designates a receiving node to receive responses to the probe, and wherein the receiving node is the first node responsive to the transaction having a first type, and wherein the receiving node is the second node responsive to the transaction having a second type.

35. (New) The first node as recited in claim 34 wherein the probe comprises a packet including a command field identifying the packet as the probe, and wherein the indication is included within the command field.

36. (New) The first node as recited in claim 34 wherein the first type is a write of a first number of bytes, the first number of bytes being less than a second number of bytes in a cache block of data.

37. (New) The first node as recited in claim 36 wherein the second type is other than the write.

38. (New) The first node as recited in claim 34 wherein the probe comprises a first packet including a target node field identifying the first node and a source node field identifying the second node.

39. (New) The first node as recited in claim 34 wherein the circuit comprises a memory controller configured to communicate with a memory in which the cache block is stored, and wherein the memory controller is configured to generate the probe in response to selecting the request to access the memory.

40. (New) A computer system comprising a plurality of nodes coupled via a plurality of links, wherein the plurality of nodes are configured to participate in a transaction, and wherein a first node of the plurality of nodes is a source node of the transaction configured to generate a request, and wherein a second node of the plurality of nodes is a target node of the transaction and is coupled to a memory including a cache block addressed by the transaction, and wherein the second node is configured to generate a probe in response to the request, wherein the probe includes an indication which designates a receiving node to receive responses to the probe, and wherein the receiving node is the source node responsive to the transaction having a first type, and wherein the receiving node is the target node responsive to the transaction having a second type.

41. (New) The computer system as recited in claim 40 wherein the probe comprises a packet including a command field identifying the packet as the probe, and wherein the indication is included within the command field.

42. (New) The computer system as recited in claim 40 where a third node of the plurality of nodes is coupled to receive the probe.

43. (New) The computer system as recited in claim 42 wherein the third node is configured to generate a probe response, and wherein the third node is configured to route the probe response responsive to the indication.

44. (New) The computer system as recited in claim 40 wherein the second type is a write of a first number of bytes, the first number of bytes being less than a second number of bytes in a cache block of data.

45. (New) The computer system as recited in claim 44 wherein the first type is other than the write.

46. (New)The computer system as recited in claim 40 wherein the probe comprises a first packet including a target node field identifying the target node and a source node field identifying the source node.

47. (New) The computer system as recited in claim 46 further comprising a third node coupled to receive the probe and generate a probe response in response to the probe, and wherein the probe response comprises a second packet including a response node field, and wherein the third node is configured to use a value from the target node field of the first packet as the value in the response node field responsive to the indication designating the target node as the receiving node.

48. (New) The computer system as recited in claim 47 wherein the third node is configured to use a value from the source node field of the first packet as the value in the response node field responsive to the indication designating the source node as the receiving node.

49. (New) The computer system as recited in claim 40 wherein the second node comprises a memory controller configured to communicate with a memory in which the cache block is stored, and wherein the memory controller is configured to generate the probe in response to selecting the request to access the memory.